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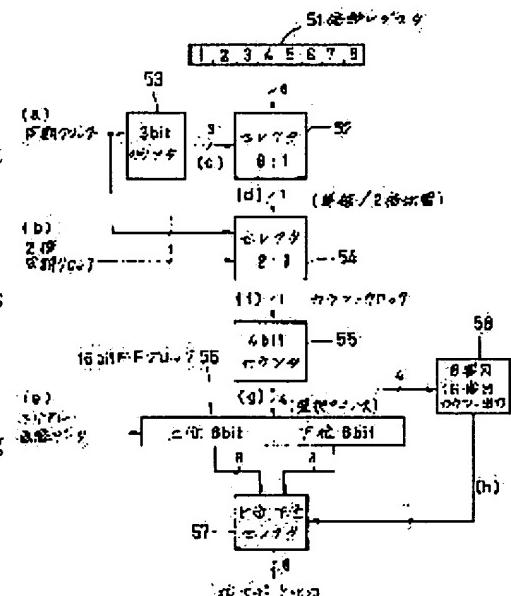
**(54) IMAGE DATA MAGNIFICATION PROCESSOR**

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**(57) Abstract:**

PURPOSE: To obtain an image data magnification processor capable of performing magnification processing without once storing transferred image data.

CONSTITUTION: A selector 52 inputs a bit in sequence in accordance with the count value (C) of a 3-bit counter 53 out of data of eight bits from a magnification register 51 to a selector 54. The selector 54 outputs a synchronizing clock (a) when inputted magnification register value output (d) shows zero, and a twice synchronizing clock (b) when it shows one as a count clock (f) to a 4-bit counter 55. The 4-bit counter 55 outputs a selection address (g) to a 16-bit FF block 56 synchronizing with the count clock (f). The 16-bit FF block 56 latches serial image data (e) at the input timing of the selection address (g). A high-order/low-order selector 57 outputs magnification data of eight bits by switching the high-order eight bits and low-order eight bits of the 16-bit FF block 56.



**LEGAL STATUS**

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